Appendix D

English Translation of Japanese patent publication 61-236284 of Kirimoto

(19) Japan Patent Office (JP) (11) Unexamined Patent Application Publication

(12) Japanese Unexamined Patent Application Publication (A) S61-236284

(51) Int. Cl.[4]	Identification symbols	Internal file number	(43) Published October 21, 1986
H04N 7/087		7013-5C	
7/08		7013-5C	

Request for examination: Not filed Number of inventions: 1 (5 pages total)

(54) Title of invention Character Signal Receiver

(21) Japan Patent Application S60-77618
(22) Filed 12 April 1985

(72) Inventor	Kirimoto, Masao	c/o Matsushita Electric Industries Co., Ltd. No. 1006, Oaza Kadoma, Kadoma City
(71) Applicant	Matsushita Electric Industries Co., Ltd.	No. 1006, Oaza Kadoma, Kadoma City
(74) Agent	Patent Attorney Nakao, Toshio	and 1 other

SPECIFICATION

1. Title of the Invention

Character Signal Receiver

2. Claims

A character signal receiver, comprising a code detecting means for detecting a specific code of a character signal superimposed on a horizontal scan period within a vertical blanking period of a television signal, a code memory in which an output of said code detecting means is written, an address generating means for counting said horizontal scan periods, a means for writing an output of said code detecting means to said code memory to an address set by an output of said address generating means, a vertical synchronizing signal drop detecting means for outputting a drop signal if said vertical synchronizing signal is not detected in a fixed period, and an arithmetic control means for reading first data written to said code memory in an initial state and reading second data written to said code memory in accordance with output of said vertical synchronizing signal drop detecting means, wherein the occurrence or non-occurrence of a channel switching in which said character signal is sent out is determined by comparing said first data and said second data.

3. Detailed Explanation of the Invention

Field of Use in the Industry

The present invention relates to a character signal receiver.

Prior Art

Character broadcasting is a broadcasting system that transmits image data constituted by characters and figures in weather forecasts, news, stock information, and the like, as digital data signals. Character signals are superimposed in the fields following the tenth horizontal scan period (10H to 21H) of the vertical blanking period of a television signal from 273H to 284H. Character signals are transmitted in data packets with one horizontal scan line as unit as shown in Fig. 5. In Fig. 5, (A) is a horizontal synchronizing signal, (B) is a color burst, (C) is a data packet constituted by 37 bytes, and in data packet 3, (D) is the first 3 bytes, being a synchronizing part, and (E) is the remaining 34 bytes. Furthermore, in the synchronizing part 4, (F) is the two bytes, "1010101010101010," which is called clock run-in (CRI) and is for used bit synchronization, and (G) is the one byte, "11100101," which is called framing code and is used for byte synchronization.

Generally, when character signals are received with a character broadcast receiver, it is done by extracting a program number from the transmitted programs and storing the extracted program number in a program number memory of the receiver. Accordingly, the receiving person can select the character broadcast program presently being transmitted by displaying data stored in this program number memory on a screen. However, when data is once stored in the program number memory, that content is preserved until the power to the receiver is cut, and therefore when one switches from a certain channel that is providing character broadcast to another channel, the character broadcast program number of the previous channel remains in the program number memory. Because of this, after the receiving person has switched the channel, one must cut the power to the receiver or delete the content of the program number memory, and it is inconvenient in operation.

In the past, a method in which an output of detection of the framing code of character signals is monitored and the program number memory is cleared at the point when disappearance of that output of detection is sensed in a prescribed period has been proposed (for example, the publication of Japanese Unexamined Patent No. S58-137376). Fig. 6 shows the configuration of the main elements of a character signal receiver in one working example of the conventional art. In the same drawing, a framing code detection pulse (FCD) is connected to one input of a NAND gate circuit 11 via a framing code detection pulse input terminal 10. Also, a signal gate pulse (CG) is connected to another input of said NAND gate circuit 11 via a signal gate pulse input terminal 12, and also is connected to an input of a counter 13. An output of said NAND gate circuit 11 is connected to a reset input of said counter 13, and also is connected to a reset input of JK-FF14. An output of said counter 13 is connected to a clock input of said JK-FF14, and a clear output signal (SD) is extracted from the output via a clear output signal terminal 15. Fig. 7 shows signals of each circuit component in Fig. 6. A clear output signal is generated after a fixed time from disappearance of the framing code detection.

Problems the Invention Attempts to Solve

In such conventional circuit, if character broadcasting service is not provided by a switched channel when another channel is switched, there is a possibility that the framing code detection output may occur unchanged and the program number memory may not be cleared.

The present invention was created in consideration of such point, and it provides a character broadcast receiver having a function that clears the program number memory regardless of the presence or absence of a character broadcasting service when another channel is switched.

Means for Solving the Problems

The present invention is a character signal receiver, comprising a code detecting means for detecting a specific code of a character signal superimposed on a horizontal scan period, a code memory in which an output of said code detecting means is written, an address generating means for counting said horizontal scan periods, a means for writing an output of said code detecting means to said code memory to an address set by an output of said address generating means, and an arithmetic control means for reading data written to said code memory in an initial state and reading data written to said code memory if a vertical synchronizing signal is not detected in a prescribed period.

Operation

It is determined as to whether or not a channel was switched, by comparing the content of the code memory in the initial state and the content of the code memory at the point when a vertical synchronizing signal was not detected in a fixed period, and comparing the position and frequency of superimposition of a character signal.

Working Examples

Fig. 1 shows one working example of the present invention. In the same drawing, a clock signal synchronized with a character signal is supplied to a clock input of a code detecting means 20 via a clock signal input terminal 21, and the character signal is supplied to a character signal input of said code detecting means 20 via a character signal input terminal 22. A horizontal synchronizing pulse is supplied to a reset input of a latch circuit 24 via a horizontal synchronizing pulse input terminal 23, and also is supplied to a count input of an address generating means 25. A vertical synchronizing pulse is supplied to a reset input of said address generating means 25 via a vertical synchronizing pulse input terminal 26, and also is supplied to an input of a vertical synchronizing signal drop detecting means 27. An output of said code detecting means 20 is connected to an input of said latch circuit 24. An output of said latch circuit 24 is connected to one input of a data switching circuit 28. An output of said address generating means 25 is connected to one input of an address switching circuit 29. A data input of an arithmetic control means 30 is connected to another input of said data switching circuit 28, and an address output of said arithmetic control means 30 is connected to another input of said address switching circuit 29.

A character signal superimposition section gate signal (PG) is supplied to another input of said data switching circuit 28 via a PG input terminal 31, and also is supplied to another input of said address switching circuit 29. An output of said data switching circuit 28 is connected to a data input of a code memory 32, and an output of said address switching circuit 29 is connected to an address input of said code memory 32. An output of said vertical synchronizing signal drop detecting means 27 is connected to an input of said arithmetic control means 30, and a channel switching detection signal is output via a channel switching detection signal output terminal 33.

Below, the operation of the present working example is explained while referring to Fig. 2. In the same drawing, (H) is a waveform of the PG supplied via said PG input terminal 31, (I) is the horizontal synchronizing pulse supplied via said horizontal synchronizing pulse input terminal 23, and (J) is the vertical synchronizing pulse supplied via said vertical synchronizing pulse input terminal 26. During a period when the PG is low level, the output of said address generating means 25 and the output of said latch circuit 24 are added to said code memory 32, and they are not connected to said arithmetic control means 30. During a period when the PG is high level, the output of said data switching circuit 28 and the output of said address switching circuit 29 are switched to the side of said arithmetic control means 30, and therefore this arithmetic control means can read the content of said code memory 32.

Now, if a character signal is transmitted in a state such as (K), said latch circuit 24 outputs a signal (L), this output signal is added to the data input of said code memory 32, and content as shown in Fig. 3(a) is written to this code memory 32. Furthermore, in said period when the PG is high level, said arithmetic control means 30 reads the content of said code memory and stores it in an internal memory.

Next, when the channel is switched and a character signal (M) is received, said latch circuit 24 outputs a signal (N), and the content of said code memory 32 changes to a state as shown in Fig. 3(b). Also, the output of said vertical synchronizing signal drop detecting means 27 is added to said arithmetic control means 30, this arithmetic control means 30 reads the content of said code memory 32, and compares it with the content of said code memory 32 stored in advance in the internal memory. In the present case, because the contents do not match, it is determined that the channel was changed, and said arithmetic control means 30 outputs a channel switching detection signal from the channel switching detection signal output terminal 33. The means of said arithmetic control means 30 in the present working example described above is shown in Fig. 4.

Effect of the Invention

According to the present invention, channel switching detection is assuredly performed if one switches from a channel providing character broadcasting service to a channel not providing character broadcasting service, and if there is a change in the position and frequency of superimposition of a character signal even if the switched channel provides character broadcasting service. In particular, in an adapter-type character broadcast receiver having a 21-pin multiconnector defined by the Electronic Industries Association of Japan, because a channel switching signal cannot be sent, the present invention is extremely effective in an adapter-type character broadcast receiver.

4. Brief Explanation of the Drawings

Fig. 1 is a circuit configuration diagram of a character signal receiver in one working example of the present invention, Fig. 2 is a timing chart for explaining the circuit operation in Fig. 1, Fig. 3 is a drawing showing the contents of the code memory in Fig. 1, Fig. 4 is a flow chart showing the operation in Fig. 1, Fig. 5 is a composition diagram of a character signal, Fig. 6 is a circuit configuration diagram of a conventional character signal receiver, and Fig. 7 is a timing chart for explaining the circuit operation in Fig. 6.

3: Data Packet, 6: Clock Run-In, 7: Framing Code, 20: Code Detecting Means, 21: Clock Signal Input Terminal, 22: Character Signal Input Signal, 23: Horizontal Synchronizing Pulse Input Terminal, 24: Latch Circuit, 25: Address Generating Means, 26: Vertical Synchronizing Pulse Input Terminal, 27: Vertical Synchronizing Pulse Drop Detecting Means, 28: Data Switching Circuit, 29: Address Switching Circuit, 30: Arithmetic Control Means, 31 PG Input Terminal, 32: Code Memory, 33: Channel Switching Detection Signal Output Terminal.

Name of Agent: Attorney, Toshio Nakao, 1 other

[see source for figure]
Fig. 1
20: Code Detecting Means
24: Latch Circuit
25: Address Generating Means
27: Vertical Synchronizing Pulse Drop Detecting Means
28: Data Switching Circuit
29: Address Switching Circuit
30: Arithmetic Control Means
32: Code Memory

[see source for figure]
Fig. 2
H 10H 21H
I
J
K Character Signal Television Signal
L
M Character Signal
N

[see source for figure]
Fig. 3